

The Simulating Annealing Algorithm for the Optimization of the Power Dissipation of the Input Test Sequences

Ramzi Zouaoui

University of Tunis El Manar
Faculty of Mathematical, Physical and Natural Sciences
LIPAH,LR11ES14
Tunis, TUNISIA
Email: zouaoui_ram [AT] hotmail.fr

Imen Herzi

Department of computer technologies,
Higher Institute of Technological Studies ISET Nabeul,
LIPAH,LR11ES14
Nabeul TUNISIA

Abstract— In this paper a new approach for solving the problem of the optimization of the power dissipation under test sequence application is proposed. This approach is based on the redundancy of test sequences and consists of the steps: redundant test generation, evaluating power dissipation for generated test sequences and construction subset of sequences with optimal parameters. The last stage is the task of the combinatorial optimization and its solution is based on the simulating annealing algorithm. Also we give the results of the computer experiments on the ISCAS-89 benchmark circuits that shows the effectiveness of the propose approach.

Keywords- sequential circuits, test generation, diagnostic redundancy, simulating annealing algorithm, power dissipation.

I. INTRODUCTION

The requirements of the electronic market push manufacturers to produce products with minimal consumption of electric energy, which corresponds to the current trend towards reducing the consumption of all forms of energy by humanity.

Digital technology is well known [1], is that peak consumption occurs during the start of the test, because right now we involve the largest (maximum) part of the logic device (circuit). In addition to the entire test and its heat dissipation parameter, one of the most commonly used indicators in assessing the quality of diagnostic input sequences is presented.

To solve the problem of constructing a test with minimal heat dissipation, several approaches have been proposed. Among them, the famous adaptation algorithms in which were introduced additional restrictions. For example, in [2] was introduced a test generator based on the algorithm PODEM wherein assigning values for undefined lines occurs so as to minimize the number of events (activities). In [3] the same

objectives are achieved at the expense of the order of input vectors in a pre-built test.

Recently, to solve many technical diagnostics problems generally we adopt non-deterministic methods such as genetic algorithms [4-5]. This is due to the inadequacies of the classical methods based on the transformation of a Boolean representation of the scheme [6], or on the construction of a decision tree [7] in which memory overflows occur, which makes them practically inapplicable to the actual size of today's digital devices.

Recently, the authors have actively started studying a new strategy optimization "SA annealing simulation." However, from the domain of metallurgy [8], retaining its initial characteristics, it was developed as an optimization approach in [9]. The strategy itself appears conceptually more transparent and easier to implement in comparison with genetic algorithms. This is due to the fact that it represents an evolution (improvement of the properties for the realization of the complete solution) which potentially occurs for the individually chosen solutions. This allows the algorithm to break free from cumbersome procedures for handling construction of the population. For the approval (validation) of the optimized properties of this strategy, the authors have already built on its basis a single-level algorithm for the generation of initialization sequences [10] and have demonstrated its effectiveness.

In this paper, we propose a 3-step approach for the construction of tests with minimal thermal dissipation based on the concept of test redundancy (excessive test). Its peculiarity is that the algorithm, to choose the optimal set of sequences in the third phase uses the new strategy of annealing simulation.

This paper is organized as follows. In the introduction we have shown the relevance of the other works (contributions) and our relationship with them in this sense. In the first section

we describe the formal declaration of proposed problem and the steps of resolution. The second part will be devoted to the description of the simulation annealing algorithm choosing optimal subsets of the input sequences. In the third section we present the results of experiments with the implementation of the algorithm. At the end, some conclusions are drawn and highlighted the prospects and possible future research.

II. THE GENERAL APPROACH FOR SOLVING THE PROBLEM

The model chosen in our work uses synchronous sequential circuits with a minimal delay of the propagation of the defects and of the physical implementation (implementation) using CMOS technology .

The goal of the work is to develop an algorithm that builds input sequences for testing with minimal thermal dissipation.

The realization of this task is performed in three steps:

- a) Excessive generation to cover the faults and defects of the input sequences.
- b) Evaluation of the quality of the solution for each of these sequences.
- c) Search for the optimal part of the input sequences.

The first two stages are two preparatory steps, while the third is to the resolution of combinatorial optimization using simulated annealing algorithm.

For the formal declaration of the problem, we define the redundancy of the input sequences of the tests.

A. Definition 1

The fault f is detected (verified) by the given sequence S with a redundancy r , if there are at least r sequences S_i with

which control the fault f . Thus r is called a redundancy factor. Here F_{const} is compressed by the equivalence of the set of simple defects having a single constant.

B. Definition 2

The test input sequence has full redundancy r , if each fault in F class checks the sequence r at least once.

C. Definition 3

The excessive plenitude of the sequence with redundancy r is equal to:

$$\text{---} \quad (1)$$

where n : it is the number of defects of the set F which is verified at least r times with the aid of the given input sequence.

Step 1: Solving the problem consists of constructing an input sequence (set of sequences) $S = \{S_1, S_2, \dots, S_l\}$ that includes excessive fullness necessary with a fixed redundancy r . Furthermore, for each fixed defect of

there is guaranteed the existence of at least r input sub-sequences belonging to S such that each of them detects this defect. The guarantee of redundancy for certain defect will then allow depending on the purpose of the job task to choose the best sequence.

Step 2: This step is dedicated to the evaluation (calculation) of the energy dissipation estimates $E(S_i)$ for each subsequence

. The problem is actually in the simulation of the circuit at a given input sequence and obtaining on this basis the necessary data.

The indicator of the dissipation of the thermal energy with the simulation of a given input sequence S_{input} largely depends on the technology of the physical realization of the microcircuits. Currently, the most common production technology for microcircuits (chips) is CMOS. The activity of the simulated circuit due to the application of the given input sequence influences only the dynamic component of the thermal dissipation when the static part does not depend on it. It is also known that the dynamic component of thermal dissipation is dominant.

It is known in [11] that the CMOS technology for power dissipation and for a given input sequence is determined by the following expression:

$$(2)$$

where V : the voltage of the circuit, C : the physical capacitance of the output valve, f : the operating frequency of the circuit and N : the number of events in the simulation to a given input sequence.

Thus, to estimate the power of the heat dissipation from the accuracy to the exact coefficient, we must calculate the parameter P which in turn admits the following representation:

$$= \quad (3)$$

where L : the length of the input sequence (the number of input vectors) and the activity of the valve is determined by the expression:

$$(4)$$

Performing the $A(S_{input})$ parameter calculation allows us to make any event modeling algorithm that works with faulty circuits. To solve this problem, previously, the authors described the algorithm [12] with propagation signal delays.

III. THE SIMULATED ANNEALING ALGORITHM FOR THE SELECTION OF THE SET OF SUBSEQUENCES

Step 3: On the basis of the SA algorithm, we involve the selection (choice) of the subset of sequences so as to satisfy the following two conditions:

$$(5)$$

$$(6)$$

Let's take an example that reveals the heart of the stage. Suppose that for some circuits (schema) the set of testable defects, the test sequence, where the subsequences, have the following characteristics:

Suppose in the possible solutions we use the following subset S :

and

Let us list the characteristics of these sequences:

From the calculations, it is clear that we must exclude the series from the list of potential solutions since it represents worse (lower) properties than those of the other series. Among the remaining set of series with better properties, we must choose the one that admits the lowest dissipation parameter,

namely, S_1 . Thus, from the example we see that the set is excessive and from this set, without the loss of its integrality, we can exclude either the sequence S_4 (energy dissipation = 73) or the sequence S_6 (energy dissipation = 88) although in these cases the fullness of the tests is 100% whereas their power dissipation parameter is higher than that in the other cases and this set will not be chosen as optimal.

Let us present some basic concepts that will be necessary for the description of the strategy (algorithm) of the annealing simulation. This strategy is presented as an iterative algorithm for improving the properties of a potential solution. For each step i of the algorithm, a configuration is associated and each function corresponds to a function which indicates the quality of this configuration from the point of view of the resolution of the problem, this is the cost function C_i . In addition we have introduced modification operations which make it possible to construct an environment (a concept) that is only a set of points with altered characteristics. The calculation of the evaluation function for the points of the environment can show the degradation of their quality in relation to the starting point. The acceptance or rejection of such deterioration is demonstrated by the temperature distribution $\{T_i\}$. The purpose of the construction of this distribution is that, with high temperatures, the probability of choosing the worst solution is higher than at low temperatures. The choice of the temperature distribution defines the cooling rate of the substance and thus significantly influences the search results.

On this basis we give a brief description of the annealing simulation algorithm:

1) The algorithm starts with the construction of its initial configuration $K_i = K_1$ and its cost $C_1 = C(K_1)$. Also for the distribution of temperatures we choose the initial temperature $T_i = T_1$. The following steps of the algorithm are repeated iteratively until the solution is found or until the maximum number of iterations is reached.

2) For the current temperature T_i and by applying the modification operations on this configuration K_i , builds its environment composed of N configurations K_i

3) For each configuration K_i of the environment O_i it computes its cost $C_i = C(K_i)$ as well as the cost improvement parameter $\Delta C_i = C_i - C_i$, the changes made as a result of the disruption, or will be accepted, or rejected if the change in the cost function is negative, so the intermediate configuration replaces the current one. Otherwise, such a change will take place on the basis of the Boltzmann distribution:

where k - a Boltzmann heuristic constant

4) By incrementing the iteration counter $i = i + 1$, the current temperature changes according to the chosen temperature distribution: $T_{i+1} = \text{actualiser}(T_i)$.

5) Go to step 2.

In the quality of the configurations in the proposed algorithm, it acts the set of numbers of the subsequences of S which in fact define the input sequence. The numbers in different configurations vary during the evolution as well as their number, but we will not take into consideration the order of the numbers in the configurations.

Three conventional disturbance operations for sets are used: modification, deletion or addition of any element. The choice between the types of operations is also random.

The algorithm is divided into two phases, and in each phase applies its own cost function.

In the first phase, subsets will be selected from S , each of which satisfies the following condition:
namely, the subsequences included in the set S' all show the non-maintainability dismantled by the sequences of S . In this case, the evaluation function is then given by:

(8)

As soon as the set of subsequences that satisfy the condition (5) is discovered, the SA algorithm immediately proceeds to phase 2 for the optimization of this set. In the second phase, the configurations are developed in such a way as to reduce the dissipation of heat for the subset of the sequences and the evaluation takes the form:

(9)

where $E_{max} = E(S)$. Thus the disturbance operations which lead to the violation of condition (5) are considered non-corrective.

The efficiency of the SA algorithm is measured by the decrease in heat dissipation for the input and output configuration of phase 2.

Note that since for a single temperature distribution, two different cost functions will be used for the different phases of the resolution, then it is necessary experimentally to choose two values of Boltzmann constants.

IV. THE EXPERIMENTAL DATA

For 3-step algorithms, the authors solved their problems by implementing a programming (software or application). The first step in the construction of redundant test sequences has been adapted to that described previously by the authors of the genetic algorithms for the construction of the tests [13]. The modifications relate to this code fragment, in which determines the effect of the modeling fault on this input set. In the modified version of the algorithm for the assignment of the defect in modeling, first we have established a requirement that the fault has been tested at least r times with r : this is the redundancy parameter. In addition, the original test generator constructed a sequence without fixing within independent subsequences. Our algorithm uses this important information. Therefore, in the data structure that stores the test sets, a change has been imported by setting the cycle time for the test sequence in which the subsequences begin.

In the second step, we proposed an adaptation to the old proposals of event modeling algorithms for fault-based digital circuits [12].

In the results of the job, a file was constructed that contains the following information:

- The total number of sub-sequences;
- The total number of defects in the compressed list;
- Then, for each sequence: the length, the number of events of the modelization, a list containing the numbers of the tested defects.

The third step was devoted to the programming and implementation of the SA algorithm described above. The volume of the software is 1100 lines of code. The experiments were performed on an instrumental computer with a 2.4GHz Core2Quad processor, 2GB of RAM.

For the selection (choice) of the optimal values of the heuristic constants, a series of preliminary experiments has been carried out. To alleviate the problem and for the sake of brevity, we will not show the search steps of the algorithm for the selection of the constants. Note that for the results we have chosen the following values: redundancy parameter $r = 5$,
 ϵ , number of configurations tested for a single temperature = 450, Boltzmann constant for First step: $k_1 = 100$, the Boltzmann constant for the second step: $k_2 = 4000$, the number of iterations without improvement = 50.

TABLE I. THE EXPERIMENTAL RESULTS

Circuit Diagram	Completeness of the test, %	Reduction of heat dissipation, %	Operating Time, Sec
s298	85,71	92,02	1
s344	96,19	92,97	1
s349	95,42	91,73	1
s382	89,47	91,02	1
s386	73,95	90,77	1
s400	88,21	93,08	<1
s444	79,32	88,72	1
s526	8,65	72,53	<1
s635	0,15	54,43	<1
s641	44,75	88,91	3
s713	81,93	91,56	1
s832	48,05	89,74	4
s938	4,40	86,31	<1
s967	7,41	89,56	1
s1196	91,22	84,19	23
s1238	77,86	76,32	6
s1269	17,87	87,77	1
s1423	73,47	81,89	5
s1488	92,19	83,25	20
s1494	95,22	89,55	9
s1512	4,86	84,75	1
s2081	8,29	93,28	<1
s3271	96,57	89,60	64
s3330	66,45	88,28	5
On average		86,34	

The experiments were carried out using circuits from the ISCAS-89 international catalog [14]. The results are shown in Tab. 1. The "Reduction of heat dissipation" column includes the result for a subsequence set that performs the transition to phase 2 of the SA algorithm. In analyzing the results, we can draw the following conclusions:

- The best results, about 90% were obtained with the easily testable circuits;
- The worst results are obtained with the circuits difficult to test for which in the first step a small number of subsequences has been generated.

V. CONCLUSION

In this paper, we proposed an approach for the construction of test sequences with minimal energy dissipation. The approach consists of three successive steps: the construction of the redundant test sequence, the evaluation of the heat

dissipation for each sequence and the choice of the optimal set of sequences. To solve the problem of the third step, we proposed to use the simulated annealing algorithm. The effectiveness of the proposed approach is demonstrated with ISCAS-89 control circuits with an average reduction in heat dissipation equal to 86.34% and up to 93.28% in the best cases.

As perspectives, we can seek to use this approach to solve other problems of optimization of input sequences for example the reduction of their length.

REFERENCES

- [1] Y. Zorian, A Distributed BIST Control Scheme for Complex VLSI Devices // Proc. 11th IEEE VLSI Test Symposium, April 1993.- pp.4-9.
- [2] S. Wang, S. Gupta, ATPG for Heat Dissipation Minimization During Test Application // Proc. IEEE International Conference, October 1994.- pp.250-258.
- [3] V. Dabholkar, S. Chakravarty, Two Techniques to Minimize Power Dissipation During Test Application in Scan Circuits // IEEE Asian Test Conference, November 1994.- pp.324-329.
- [4] Goldberg D.E., "Genetic Algorithm in Search, Optimization, and Machine Learning", Addison-Wesley.- 1989.-432p.
- [5] Ю.А. Скобцов. Основы эволюционных вычислений.- Донецк: ДонНТУ, 2008.- 326с.
- [6] A. Ghosh, S. Devadas and A.R. Newton, Sequential Logic Testing and Verification, Kluwer Academic Publishers, 1992.
- [7] O.Coudert, J.C.Madre: "A Unified Framework for Formal Verification of sequential Circuits," ICCAD-90: IEEE Intl. Conf. on Computer Aided Design, Nov. 1990, pp. 134-137
- [8] N. Metropolis, A.W. Rosenbluth, M.N. Rosenbluth, A.H. Teller, E. Teller, "Equation of State Calculation by Fast Computing Mashines", J. of Chem.Phys., Vol.21, No.6, pp.1087-1092, 1953.
- [9] S. Kirkpatrick, C.D. Gelatt, M.P. Vecchi, "Optimization by simulating annealing", Science, 220, pp.671-680, 1983.
- [10] Иванов Д.Е., Зуауи Р. Алгоритм построения инициализирующих последовательностей цифровых схем, основанный на стратегии симуляции отжига // Искусственный интеллект, 2009.- №4.- с.415-424.
- [11] A. Shen, A. Ghosh, S. Devadas, K. Keutzer An Average Power Dissipation and Random Pattern Testability of CMOS Combinational Logic Networks // Proc. IEEE International Conference on Computer-Aided Design.- pp.402-407.
- [12] Иванов Д.Е., Скобцов Ю.А. Параллельное моделирование неисправностей для последовательных схем // Искусственный интеллект. – 1999. - №1. – С.44-50.
- [13] Yu.A. Skobtsov, D.E. Ivanov. Evolutionary approach to the test pattern generation for the sequential circuits // Радиоэлектроника и информатика.- 2003, №3.- с.46-51.
- [14] Brgles F., Bryan D., Kozminski K. Combinational profiles of sequential benchmark circuits // International