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Architecture for A Zero Client Based Scalable Large Format Display System

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Abstract— **In this paper, we propose a zero client based scalable LFD system architecture. The zero client, which is a kind of the remote access terminal, receives image data to control single LCD monitor through Ethernet, supporting single display panel. In order to build LFD using multiple zero client based panel, Dasiy-Chain is adopted, connecting multiple panels by using Ethernet.**

Keywords- Zero Client, Large Format Display (LFD), Virtual Desktop Infrastructure (VDI

I. Introduction

The Large Format Display (LFD) connects the multiple LCD screens to implement large display, and it is used in the advertisement such as billboards. However, most of these screen walls are very expensive and require the high performance display controller. This controller includes a high performance graphic card for displaying via HDMI or VGA interface. These traditional interfaces have restricted to transmission distance in dozen of meters. In case of large display over maximum transmission distance, the repeater should be adopted, increasing the cost of the LFD system. On the other hand, Ethernet communication supports longer distance to the data transmission, and Gigabit-Ethernet has sufficient bandwidth for LFD.

Zero client is a computer that depends heavily on a server to support computation. By connecting with a central server, it ensures that not every workstation requires its own operating system, local CPU or memory, as all software and hardware components installed on the central server. Virtual Desktop Infrastructure (VDI) allows to gain access to secure desktop environment through a central server. It delivers a powerful and secure virtual computing solution while reducing system building and maintenance costs. Vendors have developed a zero-client based display, which support streamline business IT environment with VDI [1-4].

The LFD system, which is called display wall, has been realized in different forms of various system. Rudolfs Bundulis et al. proposed video wall controlled by mini PC [5]. Subash K et al. introduced Gigabit-Ethernet based data acquisition system for imaging array [6]. High resolution X-ray images

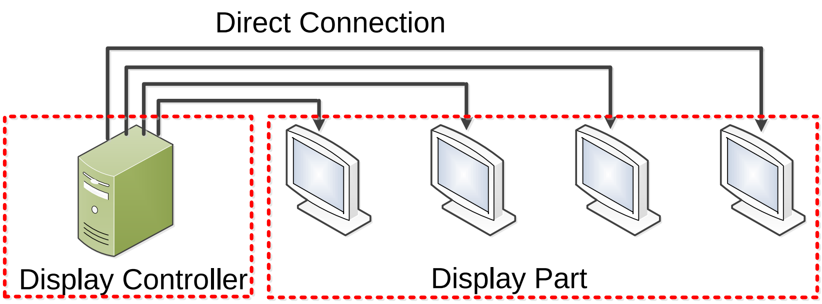

Figure 1 (a). Structure of the existing LFD system

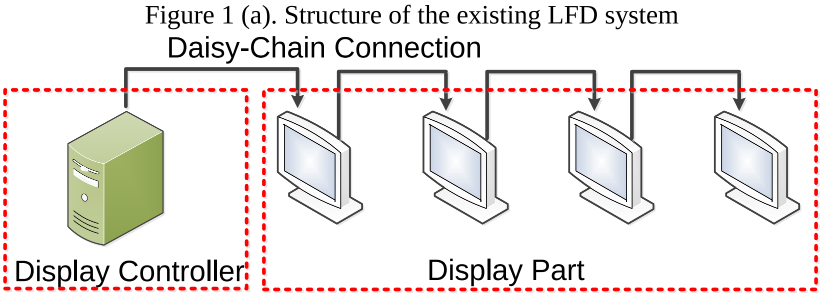

Figure 1 (b). Structure of the proposed LFD system were transmitted through Gigabit-Ethernet for image processing [7-9].

In this paper, we propose a zero client based scalable LFD system architecture. The zero client module, which is a kind of the remote access terminal, receives image data to control single LCD monitor through Ethernet, supporting single display panel. In order to build LFD using multiple zero client based panel, Daisy-Chain is adopted, connecting multiple panels by using Ethernet. We expect that our architecture efficiently realizes LFD system.

The rest of our paper is organized as follows. We introduces our system architecture including a litter core for zero client, an SDRAM controller, a Giga-bit Ethernet, and a VGA controller in section II. Section III summarizes this paper outlining the direction for future work on this topic.

II. System Architecture

Most existing LFD consists of a display part and a display controller (See Fig. 1(a)). The display part includes multiple LCD monitors and the display controller supports numerous monitor output ports in order to control the display part. Therefore, it requires a high computation power for video processing. To reduce the performance requirement, we adopted the Daisy-Chain connection to our proposed LFD system (See Fig. 1 (b)). An image display controller, which is on the display controller part, splits the image for display part, and transmits the divided image fragment with an ID. On the display part, a single zero client module controls a display monitor, and each of them is connected in Daisy-Chain using the Gigabit-Ethernet. Each zero client module has a unique module ID on the LFD system, and it enables classification of each monitor. The image data can be displayed when the received fragment ID is matched with the module ID of zero client module. Otherwise, received data is delivered to the next module through Daisy-Chain. Therefore, the image display controller does not require high performance, and Gigabit-Ethernet connection supports sufficient communication bandwidth for LFD system (See Fig. 2).

A. Little Core for Zero Client System

The Nios II core [10] is a soft core which is synthesizable for FPGA. This core is optimized for performance according to various configurations in the LFD system. One of the types of Nios II core in accordance with configurations is a Nios II/s core which is a standard core to remove a significant trade-off in software performance. This core supports the ethernet IP for Altera FPGA and has sufficient performance to manage the flow of image data. We establish two Gigabit-Ethernet channel on the FPGA because of the Daisy-Chain requires two communication channels.

B. SDRAM Controller

In order to process a large number of the image data, available memory space should be large to store image data in memory. We adopt the SDRAM as the system memory that supports sufficient memory space for managing the image data. The SDRAM memory controller can be generated by means of Qsys tool and is exploited to utilize the SDRAM in our system [11].

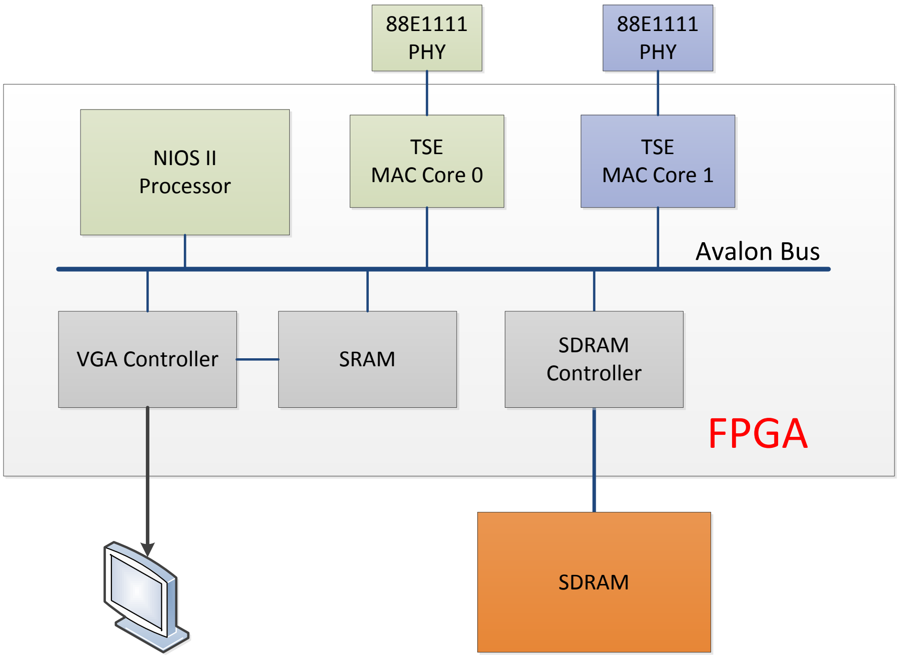

Figure 2 Architecature for a zero client module

C. Gigabit-Ethernet for Daisy-Chain

The Triple Speed Ethernet MAC (TSE MAC) IP is provided by Altera for developer who designs hardware with the Ethernet communication, and it supports 10 Mbps, 100 Mbps and 1 Gbps [12]. In our LFD system, the auto-negotiation function of Gigabit-Ethernet selects operation speed among the three Ethernet speeds. The Nios II/s core controls the operation of sub blocks such as the TSE MAC core, the Scatter-Gather Direct Memory Access (SGDMA) TX, and the SGDMA RX by setting registers of each IP. To support high-speed data transfer between a memory and the TSE MAC core, the SGDMA transfers data from system bus interconnect to streaming interface, and vice versa. In our system, two SGDMAs, which implement the role of transmitter and receiver, are connected to the TSE MAC core on the side of the streaming interface to eliminate congestion of system bus caused by massive data on the Ethernet communication. The descriptor memory includes a series of descriptors, which involve information about the data to be transferred. Because the output clock generated from the oscillator of the FPGA is not an ideal signal, the DDIO (Double Data rate Input Output) module is used for creating accurate edge-aligned transmission clock of the external PHY chip.

D. VGA Controller

The VGA controller visualizes the received data to the monitor. The VGA controller has an image buffer that stores image frame to display. We adopt the SRAM buffer to optimize the system performance, and it enables fast image display. Because the monitor display operation has the highest priority in this block, pixel buffer DMA reads data from the SRAM as soon as possible. The Nios II/s core stores an image data to the SRAM when the memory is available.

III. SUMMARY

In this paper, we introduced the architecture of our zero client based scalable LFD system. In order to build LFD using multiple zero client based panel, Daisy-Chain is adopted, connecting multiple panels by using Ethernet. We expect that our architecture efficiently realizes LFD system on an FPGA. Future work in this area is as follows. We plan to emulate the zero-client module proposed along with a server to study the performance requirement for VDI optimization. We also plan to investigate the bandwidth requirement when dealing with different workload. Last but not least, we also plan to realize the zero-client module in single chip. We expect that zero client based LFD will bring forth a new spectrum of novel usage models for displays.

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