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From device to circuit demonstrator concerning ultra submicronic Si/SiGe heterojunction bipolar transistor specified for radio frequency range systems

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Abstract— **This paper addresses a study of bipolar transistors specified for analog and analog-digital low cost circuits, working in the radiofrequency range, dedicated to popular mobiles. These devices are fully compatible with a deeply submicronic silicon CMOS technology. Advanced epitaxial growth of strained SiGe on a silicon-germanium substrate enhances the freedom for designing high speed bipolar transistors. In this process SiGe material replaces the silicon of the base of a bipolar transistor. On the theoretical point of view, numerical method for analysing hetero-structure semiconductor devices is described. Modeling and simulations have both to be performed and followed by electrical parameter extraction, and applied to an actual circuit. Low frequency noise (LFN) measurements are also presented. Often, this noise comes from different types of defects. It can be very inconvenient since, from non-linearity, it is cumbersome for circuits, systems, working with such devices in the radiofrequency range. It is worth noticing that LFN characterization is not only a useful tool to analyse complex devices, but it seems indispensable to build global compact models (Abstract)**

Keywords-component; SiGe; high-speed devices; HBTs; ECL inverter;Compact models; Noise; Silicon; Germanium

I. INTRODUCTION

The last fifteen years have seen rapid progress for the deposition of both epitaxial layers of silicon as well as pseudomorphic SiGe layers. This paper addresses SiGe epitaxial base hetero-junction bipolar transistor (HBT) technology compatible with an industrial silicon-based BiCMOS. Improving the speed of a bipolar transistor is needed for present and future communications system for low cost mass-market applications. Limitations imposed by base resistance, collector-base capacitance, punch through and breakdown voltages, for instance, are well overcame [1,4]. The Unity-current-gain cut-off frequency, f_T, is up 350 GHz, nowadays. But it seems that the presence of defects, inherent to the complex structure shrinking, is a real latch, since HBT devices is often specified to high level integration and embedded in up-to-date analog and analog-digital RF circuits. Characterisation and modelling of radiofrequency (RF) bipolar transistor such Si/SiGe devices are classical tools to analyse structures. More in-depth studies are to be extending, concerning non-ideal currents (first order) and noise (second order).

II. THE SI/SIGE SYSTEM

Employing epitaxy in device fabrication overcome the fundamental limitations of device formation by ion-implantation, namely Gaussian implantation and channelling of some species, like boron. Thermal budget of the epitaxy make abrupt impurity profiles quite difficult to be realised when the hetero-junction bipolar transistor is performed in a manner fully compatible with a standard CMOS process. To eliminate the requirement for high temperatures in surface preparation for epitaxy, UHV/CVD relying upon hydrogen passivation had been the solution. CMOS compatible silicon bipolar junction transistors (BJTs) using Si-Ge alloy for its base, are a good way to get high frequency performance, due to hetero-junctions and size reduction. The ability to engineer the band structure in semiconductors has much potential for the design of high performance devices.

In this paper, we deal with narrow-gap Si-Ge alloys. Silicon and Germanium are two crystals of carbon diamond type. They are completely miscible and their $Si_{1-x}Ge_x$ alloys have the same structure than its elements. Recalling that the lattice constant at room temperature are respectively 5.66 Å for Ge and 5.43 Å Si,

the alloy parameter verify, at room temperature, the linear Vegard's rule [5]:

$$a(Si_{1-x}Ge_x) = a(Si) + (a(Ge) - a(Si))\,x \quad (1)$$

When such an alloy layer is deposited on a silicon substrate, the mismatch may be accommodated in two ways. On one hand, if the energy embedded into the growing layer is too high, the epitaxial layer should be unstrained or relaxed, dislocations are created at the moving interface (see figure 1). On another hand, the layer can be stressed in the direction of the growth; the alloy is no more cubic, but it have a quadratic crystal structure, and we get the so called pseudomorphic epitaxial layer (see figure 2).

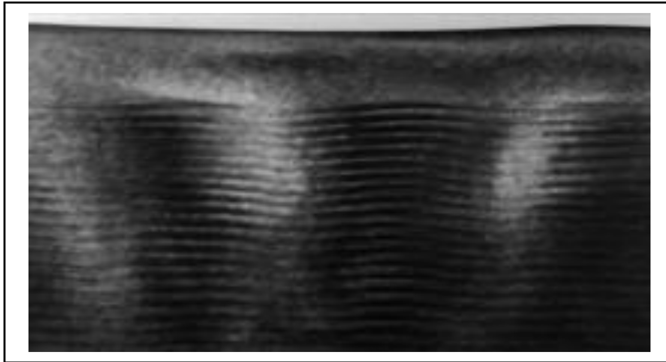

Figure 1. TEM photograh of an unstrained SiGe layer

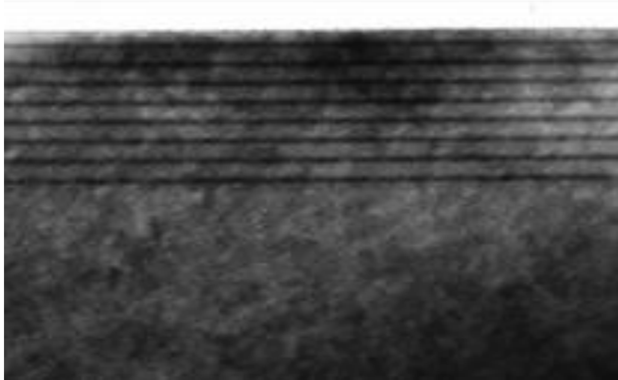

Figure 2. TEM photograh of pseudomorphic SiGe layer on a silicon substrate

A. Physical properties of strained SiGe/Si heterostructure

Strained SiGe is an indirect band gap material. The silicon bulk stress results in a modification of SiGe material band structure. A band gap narrowing occurs, compared to the raw material of same Ge composition. According to Bean [6], strained SiGe band gap (Eg) is as follows:

$$Eg(x) = Eg_{Si} - 0.96\,x + 0.43\,x^2 - 0.17\,x^3 \quad (2)$$

To solve the band alignment at the hetero-interface, it is needed to know the band gap energy of its elements, as well as the energy shift estimations (ΔEc and ΔEv). For instance, People and Bean [7] have determine ΔEv for a SiGe Growth in the <100> direction, as in

$$\Delta Ev\,(Si_{1-x}Ge_x / Si \text{ sur } Si) = 0.74\,x \quad (3)$$

The type of band alignment is driven by the determination of the conduction band ΔEc and the valence band ΔEv, respectively (see figure I.c). If ΔEc and ΔEv have opposite sign, the alignment is called type I (our case) according to People and bean, (ΔEg is always slightly higher than ΔEv). If the alloy is deposited on a $Si_{1-xs}Ge_{xs}$ substrate (xs non null), ΔEc and ΔEv have the same sign and the alignment is of type II. In the strained SiGe/Si and SiGe/SiGe, Chung and Wang [8-10] have calculated the effective mass of state density. The intrinsic concentration of the carriers depends on the bandgap, according to the relation: as in

$$ni^2 = (Nc\,Nv).\exp(-Eg/KT) \quad (4)$$

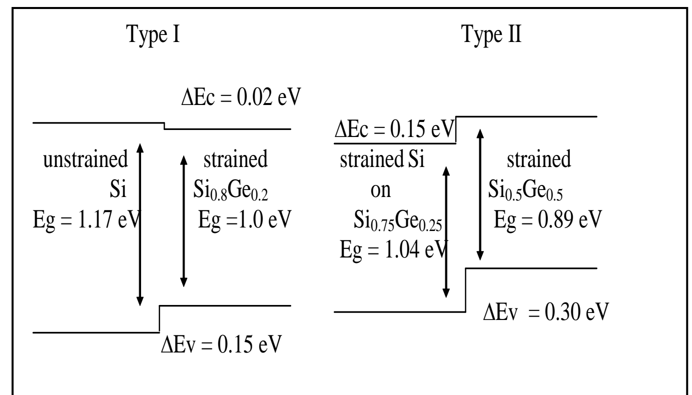

Figure 3. Schematic of energy band alignments

We have also: Eg (SiGe) = Eg (Si) – ΔEg. For a given Ge composition, ΔEg keeps constant, and we get:

$$ni^2 = (Nc\,Nv)_{SiGe}.\exp(-Eg_{Si}/KT).\exp(\Delta Eg/KT) \quad (5)$$

With respectively for the conduction band and the valence band, the effective density of states:

Then, the intrinsic concentration is affected by the Ge composition (whose ΔEg depends on); although the effective electrons mass do no vary sharply versus the stress, the hole can dramatically be modified. Meanwhile, no direct measurements have been made for electron and hole effective masses, up to our knowledge. Chung and Wang had calculated these ones, taking into account the coupling of the heavy and the light holes with the energy band.

B. SiGe HBT DEVICE DESIGN AND MODELLING

Current base (holes for NPN HBT studied below) is known to show a little or no dependence on collector-base bias. It is not affected by the SiGe presence and it is determined by the injection of holes into the emitter. Then we consider only the collector current, which can be express as:

$$Ic = \frac{q.S.\exp\left(\frac{q.V_{be}}{KT}\right)}{\int_0^{W_B} \frac{N_B(x)}{D_{nB}(x)} \cdot \frac{dx}{n_{iB}^2(x)}} \quad (6)$$

Introduction of Ge in the base offers a new degree of freedom. SiGe base increases collector current, which induces high current gain with low base resistance (because of both high doping concentration and narrow base (cf. high frequency performances, i.e. f_T and f_{max} corresponding to a reduced base transit). We present on figure 4, a TEM cross section of SiGe HBT. Thanks to a non-selective epitaxy, field oxide (cf. LOCOS) is covered with a layer of poly-Si/SiGe for contacting extrinsic base, which reduces dramatically parasitic extrinsic surfaces.

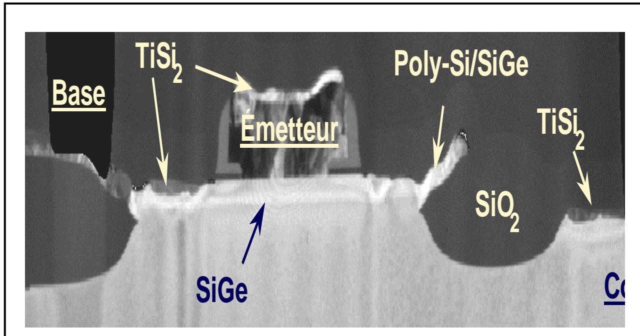

Figure 4. TEM cross section of CMOS compatible SiGe base HBT

The schematic structure is shown on figure 5. We have indicated some possible localisation of defects introduced by specific process steps (we will talk about this key problem, hereafter).

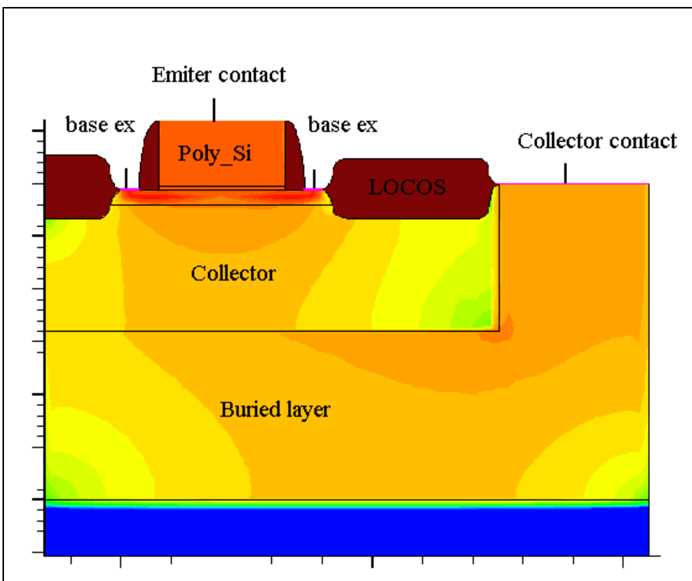

Figure 5. Schematic cross section of HBT

Finally a typical schematic shape of the relative concentrations is pointed out in figure 6; in fact, a trapezoidal Ge profile is better than linear or uniform Ge profiles, for a wide range of temperature, for transit time minimisation.

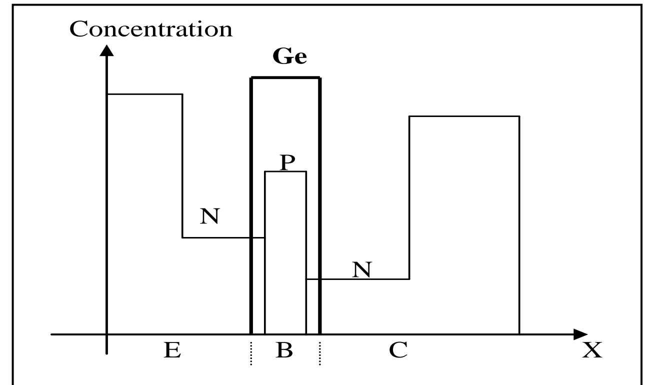

Figure 6. Schematic profile of SiGe base layer

If we consider a base doping level as constant (our simulations):

$$Ic_{SiGe} = \frac{q.S.ni^2_{SiGe}.D_{nB\,SiGe}.\exp\left(\frac{q.V_{be}}{KT}\right)}{N_{B\,\mathrm{SiGe}}.W_B} \tag{7}$$

We can evaluate the gain enhancement compared to conventional silicon bipolar transistor as follows:

$$\frac{\beta_{SiGe}}{\beta_{Si}} \approx \frac{Ic_{SiGe}}{Ic_{Si}} = \frac{ni^2_{SiGe}.D_{nB\mathrm{SiGe}}}{N_{B\,\mathrm{SiGe}}}.\frac{N_{B\,\mathrm{Si}}}{\mathrm{ni}^2_{\mathrm{Si}}.D_{nB\mathrm{Si}}} \tag{8}$$

$$\frac{\beta_{SiGe}}{\beta_{Si}} = \frac{D_{nB\mathrm{SiGe}}.(Nc.Nv)_{SiGe}}{D_{nB\mathrm{Si}}.(Nc.Nv)_{Si}}.\frac{N_{B\,\mathrm{Si}}}{N_{B\,\mathrm{SiGe}}}.\exp\left(\frac{\Delta Eg}{KT}\right)$$

In putting down:

$$\gamma = \frac{(N_C N_V)_{SiGe}}{(N_C N_V)_{Si}} \quad \text{et} \quad \eta = \frac{D_{nB}(SiGe)}{D_{pE}(Si)}$$

we can write:

$$\frac{\beta_{Sige}}{\beta_{Si}} = \eta.\gamma.\frac{N_{B\,\mathrm{Si}}}{N_{B\,\mathrm{SiGe}}}.\exp\left(\frac{\Delta Eg}{KT}\right) \tag{9}$$

γ describes the lowering of states densities due to band gap narrowing, is lesser than one.

η is greater than unity, because of the increase of the minority carrier mobility, which is as greater as Ge concentration is higher [11]. This term is beneficial for the current gain and can compensate the increase of the doping level in the base (if $Nb_{Si} < Nb_{SiGe}$). Numerical methods were first applied to heterostructure by Sutherland and Hauser to analyse solar cells [12]. A lot of other works have been accomplished, until today [13,14].

First, we briefly discuss the equations and physical model involved in the simulation of Si and SiGe BJTs as

implemented in our program, or in a commercial one. The modelling uses hereafter the so-called DDM (drift diffusion model) model, which links ambipolar continuity equations for electrons and holes and Poisson's equation. In addition, the current densities can be expressed as follows:

$$\vec{\mathbf{J}}_n = -\mathbf{n}.\mu_n.\vec{\nabla}\phi_n \qquad (10)$$
$$\vec{\mathbf{J}}_p = +\mathbf{p}.\mu_p.\vec{\nabla}\phi_p$$

The principal difference between HBT, with conventional BJT, is the presence of Si/SiGe hetero-interface at both emitter-base (EB) and collector base (CB) junctions. If Ec and Ev are normalised with the thermal voltage (U_T = kT/q), they can be written as follows:

$$\begin{cases} E_c = -\phi_0 + Eg/2 \\ E_V = -\phi_0 + Eg/2 + \Delta E_V \end{cases} \qquad (11)$$

ΔEv is the shift at the Si/SiGe metallurgical junction. In our case, we have supposed that band shift affects only the valence band, i.e:. $\Delta E_V = \Delta Eg$ and $\Delta E_c = 0$.

Experimental works have shown $\Delta E_c << \Delta E_V$ [15]. ϕ_0 is the intrinsic level.

The relations for the Fermi levels can be written as:

$$\begin{cases} \mathbf{E}_{FN} = \mathbf{E}_C + \ln\left(\frac{\mathbf{n}}{\mathbf{N}_C}\right) - \mathbf{KT}.\ln(\gamma_n) \\ \mathbf{E}_{FP} = \mathbf{E}_V - \ln\left(\frac{\mathbf{p}}{\mathbf{N}_V}\right) + \mathbf{KT}.\ln(\gamma_p) \end{cases} \qquad (12)$$

γ_n and γ_p are parameters which take into account the Fermi-Dirac Statistics. Other relations dealing with the strained SiGe/Si material are implemented in our code, such as dielectric permittivity, function of the percentage of Ge:

$$\varepsilon(x) = 11.9 + x\,(16 - 11.9) \qquad (13)$$

The band gap narrowing (BGN) is also affected by the stochiometry as: $\Delta Eg = 0.8\,x$ for $x \le 0.25$

We also consider $x = 20\%$ and $\Delta Eg = 170 - 180$ meV.

Finally, we write [16,17]:

$$Nc_{SG} = 2.8\ 10^{19} + x.\,(1.04\ 10^{19} - 2.8\ 10^{19})$$
$$Nv_{SG} = 1.04\ 10^{19} + x.\,(6.0\ 10^{18} - 1.04\ 10^{19}) \qquad (14)$$

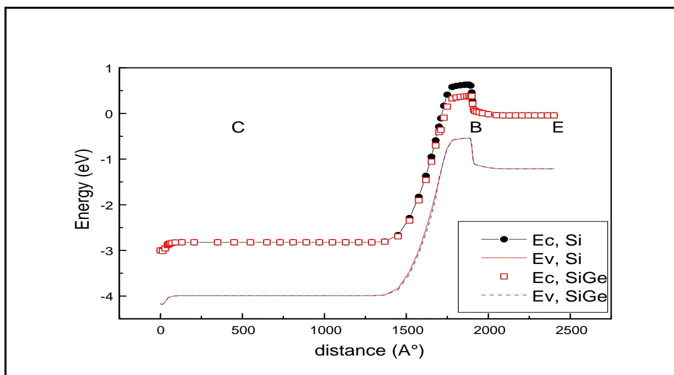

Figure 7. A $Si_{0.8}Ge_{0.2}$ HBT and its equivalent fully silicon bipolar transistor

Figure 7 shows the calculated band diagram of whole structure, which looks like quite coherent with previously explanations.

Figure 8 shows the typical Gummel characteristics of the SiGe-base transistor compared with the equivalent conventional silicon transistor (same geometry, same doping profiles).

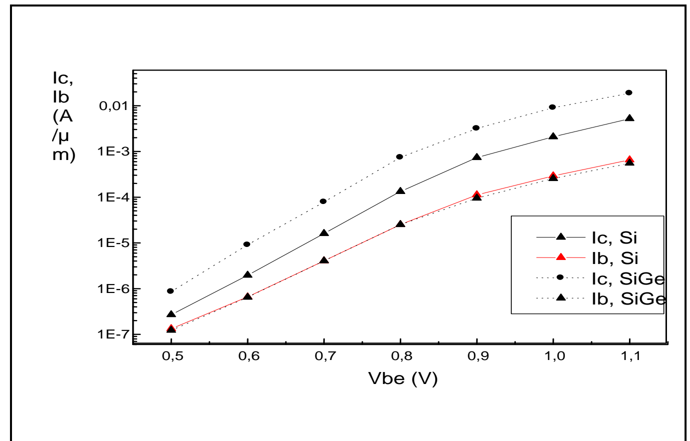

Figure 8. Gummel plots (our calculus) for the $Si_{0.8}Ge_{0.2}$ HBT and the BJT

It still confirms the model since, only the collector current is significantly increased, for the SiGe base. All these numerical calculations were done with our two-dimensional simulator. We present also on figure 9, measured Gummel characteristics which show clearly a non-ideal base current (cf. η_b), for low level injection. Identifications of defects (localisation, distribution, capture cross section) is a quite hard challenge for such sophisticated technologies. It may be located to the emitter-base and emitter-collector junctions (see noise hereafter), at the vertical interface, between the spacers and the extrinsic polysilicon emitter, due to the reactive ion etching (RIE) process step.

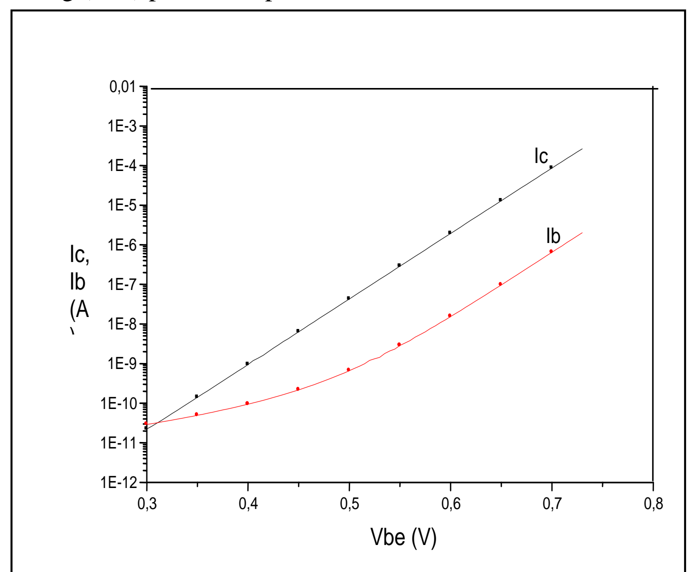

Figure 9. Typical experimental result of the HBT Gummel plot

We use an industrial simulator tool [18] to investigate these related-defects considerations. In the figure 5 are presented the Gummel plots considering there are only uniformly distributed defects along the spacers. We have extracted a non-ideality parameter for the base current up to 2.

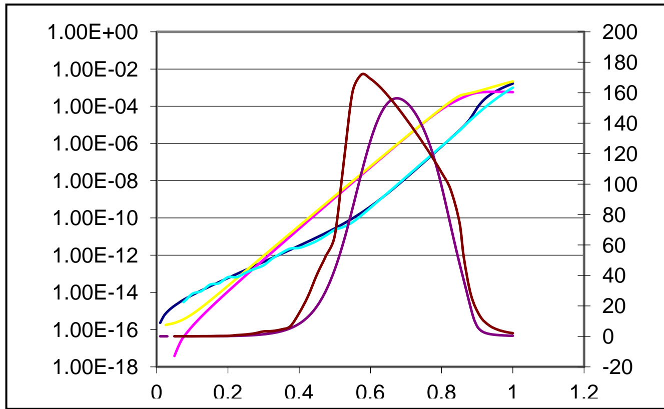

Figure 10. HBT's Gummel plots(ISE) : numerical drift diffusion model simulations compared with a SPICE simulation

The capture cross section is taken to the constant value of 10^{-13} cm^2. This latter value is high, but we got it, sometimes, although the classical value are around 10^{-17} cm^2. Capture cross section is obtained by deep level transient spectroscopy – DLTS –measurements). But, in fact, we have found that the ISE simulator is not sensitive to the defects since the capture cross section is less this 10^{-13} cm^2 value (it's the major reason for our developing DDM simulator in order to take into account the defects). Another reason to use the powerful ISE CAD tool, is the possibility to extract automatically (with some caution) some electrical circuit parameters, so called SPICE parameters – but not all , especially transit times in RF. These parameters, extracted from steady and dynamic regime, give the ability to perform RF circuit simulations.

C. DYNAMIC ELECTRICAL PARAMETERS

In most RF and microwave circuit applications, it's the transistor frequency response f_T that limits system performance. f_T depends principally on transconductance, on intrinsic depletion capacitances and carrier transit times. The unity power-gain frequency or maximum oscillation frequency (f_{max}) is a more relevant figure of merit for practical and microwave applications, since it depends not only on the intrinsic transistor performance, as f_T but also on device parasitics, e.g. the total ac base resistance. These two fundamental parameters, f_T and f_{max}, can be extracted from current and Mason gains, respectively, h_{21} and G_{MU} (at 0 dB), themselves directly calculated from S-parameter dependant formulas. These two fundamental frequencies, were presented on the figures 11, with collector current dependency Ic. They are very well fitted by our calibrated HICUM Model (via ADS).

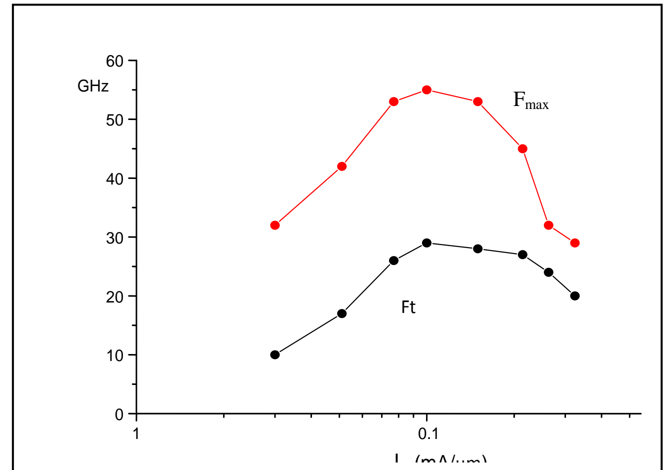

Figure 11. f_T and f_{max}

D. NOISE CHARACTERIZATION

Si/SiGe transistors with high Ge concentration in the base layer are capable of very low noise figures [19]. But this situation may be overcome by the presence of various types of defects in the HBTs, which can induce essentially low-frequency noise (LFN). There is a special interest in characterisation and modelling such a noise. First of all, it is a useful tool for evaluate process and device reliability. Moreover, LFN is up-converted towards the carrier of a RF device, such as Voltage Controlled Oscillator (VCO) designed with the HBT device because of the circuit's non-linearity (cf. Phase noise amplitude). Indeed, we ought to go further concerning defect analysis, which is a key point in such small structure. There are several noise sources (from some process step, deep levels,...) in such structures like the HBT's, independent or not. The great difficulty, by now and for the future, lies in characterising and discriminating them. For instance, in our case, we also met very peculiar noise source when studying our HBTs, which are inherent to the very reduced size of these structures. Presence of traps involves current random fluctuations at the origin of a low frequency noise, or Random Telegraphic Signals (RTS) in the HBTs. At low injection, main contributions to base current arise from generation-recombination or trap assisted tunneling process in base current. Figure 12 shows a typical I_b characteristics (part of the "Gummel"). An excess base current is observed at low injection and the ideality factor η_b is near or exceeds 1.5, for these Vbe values. Current base RTS properties is then investigated in this Vbe bias range.

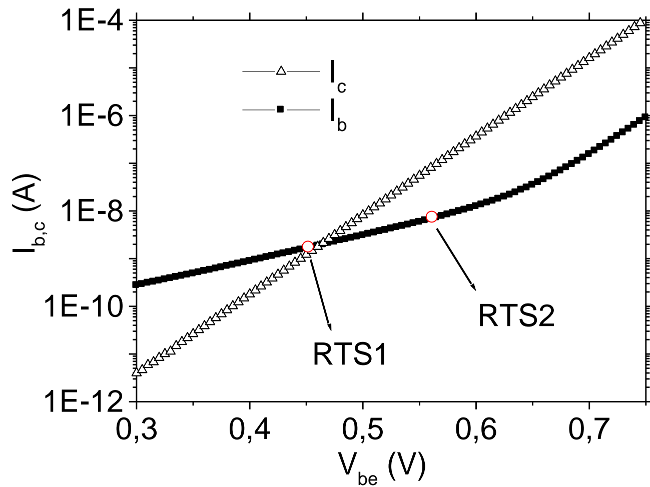

Figure 12. Non-ideal charcteristic Ib(Vbe)

Figure 13 shows a typical RTS noise observed on the base current. This current base exhibits two-level discrete fluctuations . For lower temperature (not presented here), the noise frequency decreases, indicating that the process is thermally activated. Contributions to current base can arise from generation recombination phenomena and band-to-band tunnelling, or Poole-Frankel effect. The dominant conduction process has been extracted from the temperature current dependency and implies the presence of deep traps within the band gap, near the EB junction.

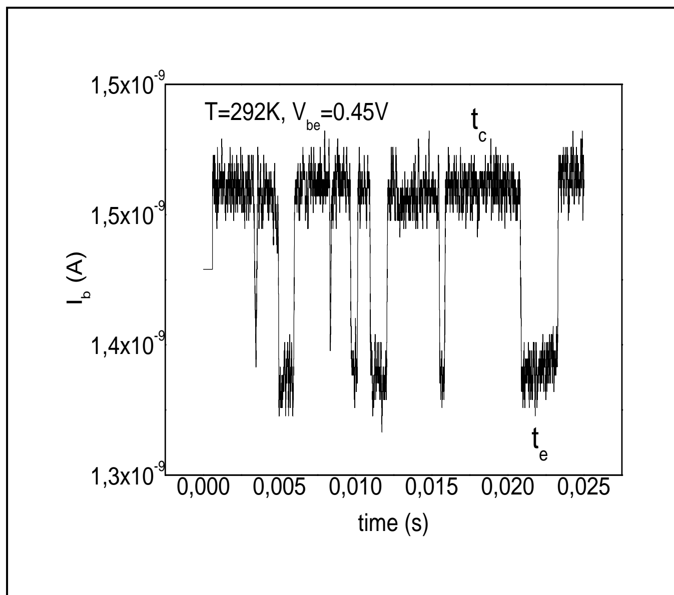

Figure 13. The associated Random Telegraphic noise, versus time, of HBT (at the emitter-base junction)

No discrete fluctuations have been observed in a region where the base current is ideal (i.e related to diffusion process). Two mechanisms could explain such current fluctuations due to deep level defects:

Local deformation of the band gap induced by trapping/entrapping of carriers on these defect [20,21]. The presence of traps, whose capture cross section of electron and hole may fluctuate randomly [22]:

$$I_{gr} = q\frac{n_i^2\left[\exp\left(\frac{qV_{be}}{k_BT}\right)-1\right]}{\frac{n(x_D)+N_C\exp\left(\frac{E_T-E_C}{k_BT}\right)}{\sigma_p\upsilon_{thp}}+\frac{p(x_D)+N_V\exp\left(\frac{E_V-E_T}{k_BT}\right)}{\sigma_n\upsilon_{thn}}} \quad (15)$$

where n_i is the intrinsic carrier concentration, $n(x_D)$ and $p(x_D)$ are respectively free electron and hole concentrations at the defect position, N_C and N_V are the effective density of states in the conduction and the valence band, respectively, σ_n and σ_p are electron and hole capture cross section, respectively, v_{thn} and v_{thp} are electron and hole thermal velocities, respectively. Two current levels are present:

high state (carrier capture) : (σ_n1, σ_p1) , I_{gr1} and low state (carrier emission) : $(\sigma_n2, \sigma_p2) = (0,0)$: approximation , I_{gr2}
Then, we get the amplitude difference $\Delta I_{BE} = I_{gr1} - I_{gr2}$ between the two levels (figure 8). Theoretical amplitude of telegraphic noise can be expressed as [23, 25]:

$$S_I(f) = \frac{4(\Delta I)^2}{(t_c+t_e)\left[\left(t_c^{-1}+t_e^{-1}\right)^2+(2\pi f)^2\right]} \quad (16)$$

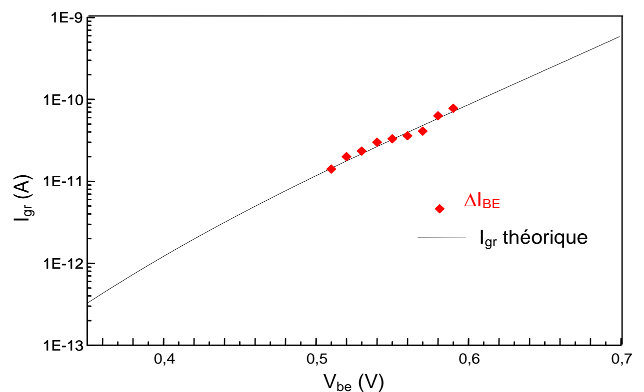

Figure 14. Random telegraphic noise magnitude (base-emitter junction)

with t_c and t_e are the average of the low and high time duration, respectively. The spectrum is a Lorentzian with a cut-off frequency f_T which verifies equation 17:

$$\frac{1}{te} + \frac{1}{tc} = 2\,\pi f_T$$

For such noise, the cut-off frequency f_T corresponds to the maximum of f . $S_I(f)$ product. A Fast Fourier Transform (FFT)-based method is applied to the time domain RTS. The technique allows us to calculate the noise spectrum and then to measure the cut-off frequency (even at very low frequencies: from 0.1 Hz), which is depending on the capture and emission time of the traps and the RTS amplitude. A typical power density spectrum (PSD) is shown on the figure 15. It can be splitted in two components – 1/f and white noise – plus an additional lorentzian noise, typical of the presence of a GR centre. This RTS measurement method is complementary with conventional LFN measurements and can be applied even for extremely low frequency.

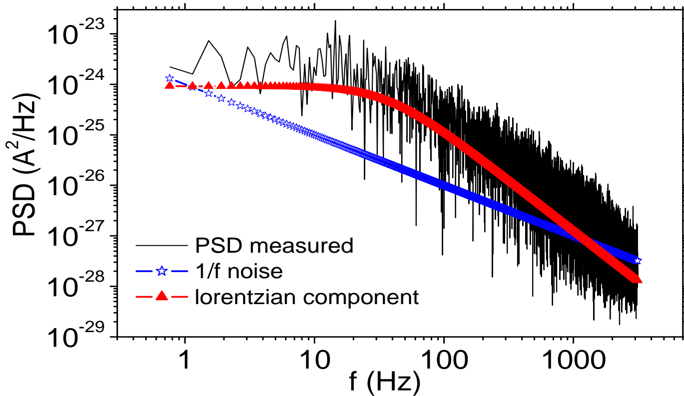

Figure 15. Noise power density (A^2/Hz) extracted from Random telegraphic noise measurements (RTS2)

E. HICUM current processes of bipolar technologies.

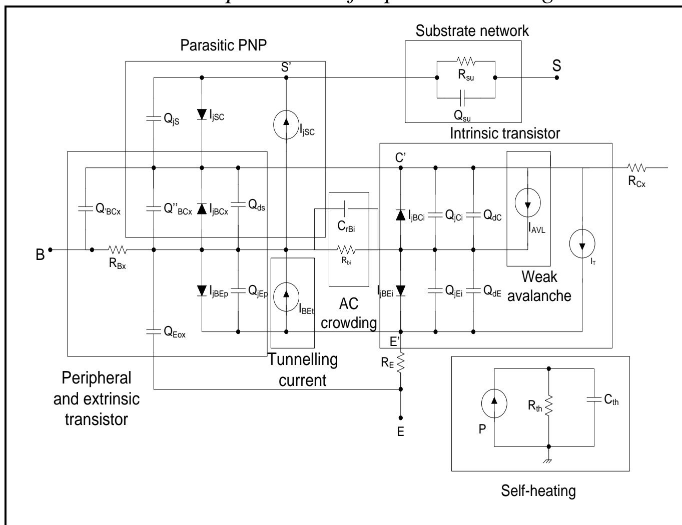

Figure 16. Electrical schematic of the HICUM Model

HICUM [26] (figure.16) is an advanced model intended for high frequencies applications. The equivalent circuit of HICUM model considers all important physical effects for the It is difficult to extract both emitter resistance RE and base resistance RB although in this technology, RE is near one Ohm, RB (especially the intrinsic one) is quite fundamental concerning the RF behavior, and is also crowding dependant; HICUM uses a current crowding factor. More generally, results obtained in our study are efficiently compared (not presented here) with electrical characteristics obtained by measurements and SPICE-like parameter extractions from simulations via essentially the compact model (HICUM) implemented in the so-called commercial simulator ADS (Advanced Design System). This point is important, since the accurate HICUM model will allow us good future design of different circuits. The conception of high speed digital and analog circuits requires an exact description of the loads, the capacitances and also transit times versus the collector polarization (I_C, V_{CE}).

III. First order electrical parameter extraction one example: ECL gate delay-time

In order to analyze ECL gate delay-time, we consider the propagation time τ_{pd} which is figure of merit that we envisage to optimize as well as dependence on frequency performance (f_T) through ideal transit time τ_F (forward-active operation). In the other side, we develop expressions (in dynamical study) for the six constant time of the SiGe HBT that restrict switching performance: R_{BX} C_{Cx} , R_L C_{Cx}, R_{Bi} C_{JE} , R_{Bi} C_{Cx}, R_{Bi} C_d, and R_{Bi} C_{BC} (extrinsic and extrinsic resistance and capacitance). Consequently, optimizing ECL gate delay-time requires the reduction of these terms [27]. We use the global expression [28] given in equation 18, where a weighted sum of various terms have been introduced in order to take into account all parameters that affect τ_{pd} .

$$\tau_{pd} = \sum K_i R_i C_i + K_j \tau_F \quad (18)$$

ECL gate delay-time is also dependent on logic swing V_L between the gate high and low state and voltage logic levels [29].

A. Circuit design

The block diagram shown in figure.17 **c**onsists of a differential pair loaded by an emitter-follower pair to reduce the loading effect of the following stage, speeds up the regeneration process, and increases the output voltage swing. In ECL technology, the operating current through a load resistance defines the maximum speed of the cell. The large load resistance (R_1, R_2 and R_3) will increase the recovery time, whereas a small will limit the output swing and degrade the gate operation.

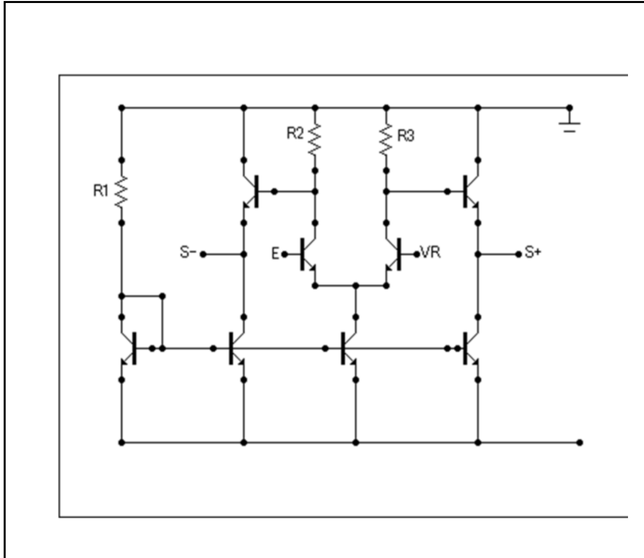

Figure 17. Block diagram of ECL inverter

SiGe HBT technology used is from self-aligned double-mesa process [30], in order to reduce the collector extrinsic capacitance C_{Cx}. An additional advantage associated with this technology is a base extrinsic resistance R_{BX} reduction. Typical electrical characteristics, geometry and doping parameters are summarized in table 1 and table 2.

TABLE I. SUMMARY OF THE SIGE HBT PARAMETERS

Emitter finger width Emitter finger lengths	0.2 µm 20.0 µm
Extrinsic base finger width Extrinsic base finger length	0.2 µm 20.0 µm
Base-collector intrinsic region area Base-collector extrinsic region area	20.0 µm² 80.0 µm²

TABLE II. TYPICAL SIGE HBT CHARACTERISTICS

Description	Parameters	Values
Ge concentration	% Ge	35
Base sheet resistance	Rsi (Ω/□)	600
Base thickness	W_B (nm)	40
Collector thickness	W_C (nm)	100
Emitter doping	N_{dE} (cm^{-3})	$3.0\ 10^{18}$
Collector doping	N_{dC} (cm^{-3})	$3.0\ 10^{17}$
Base doping	N_{aB} (cm^{-3})	$4.0\ 10^{19}$
Maximum gain	β_{max}	550
Cutoff frequency	f_T (GHz)	73
Maximum frequency	f_{max} (GHz)	55

To interpret delay time variations affected by various parameters, we based on equation (18). SiGe ECL gate delay depends strongly on the base thickness and doping concentration as illustrated in figure 3. The emitter doping profil and base thickness have been optimized for a minimum delay. The Ge concentration equal to 35 %, ensures sufficient gain (see Table II).

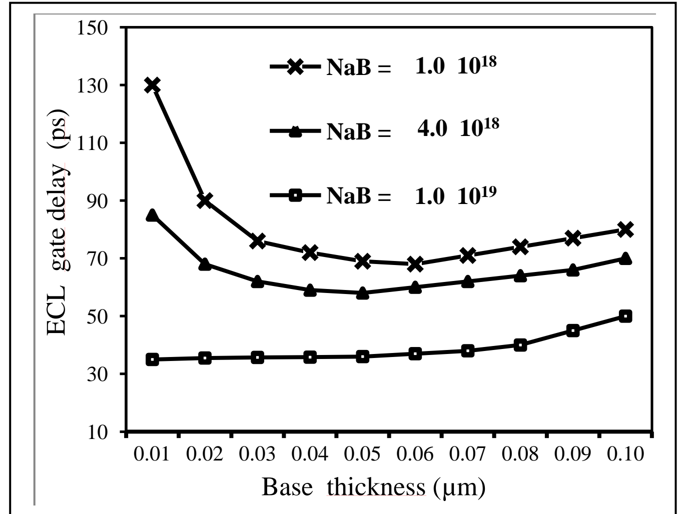

Figure 18. ECL delay versus base thickness for different values of base doping concentration N_{aB}

A minimum ECL gate delay-time of 35 ps was reached. The optimization of the gate delay is obtained for a specific value of base doping concentration, which is a compromise between high base resistance with low base thickness and high transit time with large base thickness.

B. Influence of voltage swing V_L

This parameter is firstly set at the value equal to 800 mV. The ECL delay falls when the collector current I_C increases beyond 1 mA (see Figure19), due to the low load resistance required for this V_L. This delay reached a minimum of 34.5 ps at I_C = 5 mA, when load resistance decreases but this, induced an increase in diffusion capacitance.

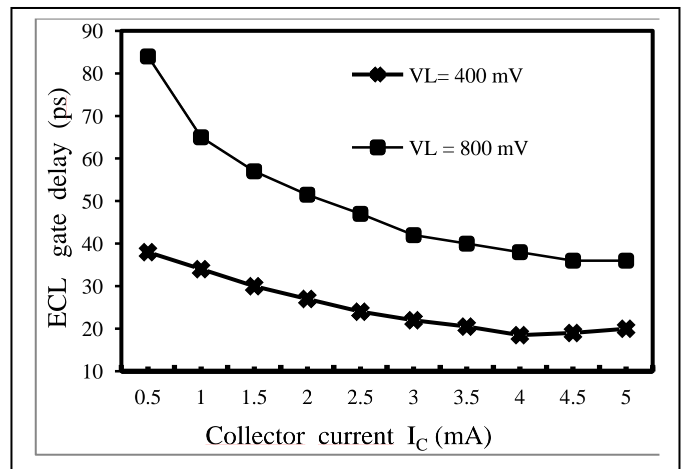

Figure 19. ECL gate delay versus collector current for two values of logic swing V_L

For V_L = 400 mV, the delay reached 18 ps but this minimum occurs at a low value of collector current (I_C = 4 mA). Indeed for this logic swing, the load resistance is half that required for V_L =800 mV.

C. Reducing device dimensions

In this section, we based the analysis on geometry and technological parameters, according to the collector current. We firstly reduced emitter finger below 1µm, with V_L = 400 mV. We observed, a significant improvement in the gate delay when the emitter finger is reduced from 1 to 0.5 µm, it consequently decreases the delay time from 16 ps to 13 ps at I_C = 5 mA (see figure 5). When this parameter is equal to 0.2 µm, a small decrease (<1 ps) is raised at high levels of collector current, however a significantly degradation is observed at low values. This behavior can be explained by considering the dominant circuit constant time (R_L C_{CX}).
When the emitter area A_E is reduced, the collector current is also reduced, consequently a greater load resistance is required to generate the given logic swing.

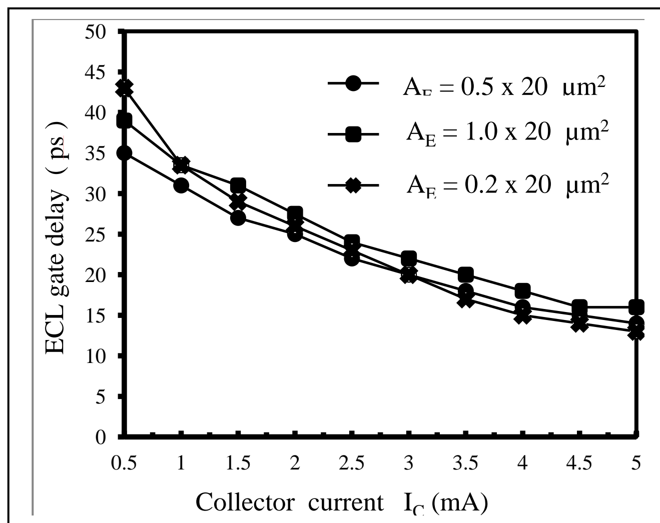

Figure 20. ECL gate-delay versus collector current for different values of emitter area A_E and with a logic swing V_L=400 mV

The load resistances may be reduced by increasing collector-current with emitter finger, which does not imply that ECL gate delay can be improved indefinitely by reducing them. Indeed, it is undesirable for ECL gate to operate at high currents levels due to high injection effects that degrade the forward transit time.
However as the extrinsic base R_{BX} is kept constant, the capacitance C_{CX} is not reduced in the same proportions.
For Ic = 5 mA, the constant time (R_L C_{CX}) became less significant, it implies an improvement of ECL gate delay for emitter finger equal to 0.2 µm, consequently, a minimum gate delay equal to 12.5 ps is obtained.

IV. CONCLUSION

The relatively recent and successful demonstrations of SiGe HBT in high performance analog and digital circuit low cost applications are the result over roughly fifteen year. During this period, process and design modelling were refined. Nevertheless, the produced impacts of these technological enhancements are still in progress. This paper can also appear as a beginning synthesis: from material to compact models. We explore HBT static and first order electrical parameters. As a circuit demonstrator, we study an ECL gate; ECL gate delay-time is derived from well-balanced transistor characteristics achieved through the fully self-aligned SiGe base structure with a fast forward transit time and low collector capacitance. Strict control at all stages of the technological process in the development of the device allows the control of all these factors, and it will be possible to optimize the switching performance. These technologies will need more and more in-depth analysis, especially for that was seeming of the second order, for a few year ago, namely due to some localised defects, fluctuations in currents or voltages, Modelling and characterisation ought to be improved. Typically, extensive low figure noise (LFN) measurements are needed to implement compact non-linear electrical models of an active device such as the HBT one. For instance, it is shown that the frequency analysis of the random telegraphic signals is a well-suited tool for the study of single defects in very small devices. It is complementary with conventional LFN measurements and extended to the very low frequency range. We will go further on extracting accurate SPICE-like parameters, both from the device simulations and for the measurements, in the static regime, followed by the dynamic one. Then the SPICE parameter sets have to be introduced into radiofrequency simulators like spectre RF (CADENCE) or ADS (AGILENT). Coupling with noise measurements, we think to improve understanding behaviour device, and perhaps to propose some methodology for the development of the next structure generations.

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